IN THE CLAIMS

1. (Currently Amended) A process for manufacturing an integrated circuit, the process comprising:

providing a substrate comprising a dielectric layer over a conductive material;

depositing a hardmask over the dielectric layer;

applying a first photoresist over the hardmask and photodefining at least one first elongated opening;

etching the hardmask and partially etching the dielectric to deepen the at least one first elongated opening to form a trench the trench having a bottom in the dielectric layer with no etch stop layer formed thereon;

removing the first photoresist;

applying a second photoresist and photodefining at least one second elongated opening transverse to the at least one trench so as to expose a portion of the dielectric defined by an intersection of the first and second openings;

etching the exposed dielectric from the bottom of the at least one trench down to the underlying conductive material.

2. (Previously presented) The process of claim 1, further comprising removing the second photoresist.

3. (Previously presented) The process of claim 1, further comprising removing the hardmask.

4. (Original) The process of claim 1, further comprising metallization and planarization.

5. (Previously presented) The process of claim 1, wherein the dielectric layer is silicon dioxide.

6. (Previously presented) The process of claim 1, wherein the hardmask is silicon nitride.

7. (Previously presented) The process of claim 1, wherein the step of etching the exposed dielectric from the bottom of the at least one trench down to the underlying conductive

material forms at least one third opening to the underlying conductive material and the at least one third opening is filled with conductive material to form a contact or a via.

8. (Previously presented) The process of claim 1, wherein the step of etching the exposed dielectric forms at least one third opening that has substantially a quadrilateral cross-section.

9. (Previously presented) The process of claim 1, wherein the step of etching the exposed dielectric forms at least one third opening that has substantially a square cross-section.

10. (Previously presented) The process of claim 1, wherein the step of etching the exposed dielectric forms at least one third opening that has substantially a rectangular cross-section.

11. (Previously presented) The process of claim 1, wherein the step of etching the exposed dielectric forms at least one third opening that has a feature size of about 0.5 micron or less.

12. (cancelled)

13. (Currently Amended) A process for manufacturing an integrated circuit, the process comprising:

providing a substrate comprising silicon dioxide dielectric layer over a conductive material;

depositing a silicon nitride hardmask over the dielectric layer;

applying a first photoresist over the hardmask and photodefining at least one elongated opening;

etching the hardmask and partially etching the dielectric to deepen the at least one elongated opening to form at least one trench, the trench forming a bottom in the dielectric layer with no etch stop layer formed thereon;

stripping the first photoresist;

applying a second photoresist and photodefining at least one second elongated opening transverse to the at least one trench so as to expose a portion of the dielectric defined by an intersection of the first and second openings;

selectively etching the dielectric from the bottom of the trench down to the underlying conductive material.

14. (Currently Amended) A method of making an integrated circuit comprising defining a via or a contact by the intersection of a first elongated opening in a first mask and a second elongated opening in a second mask transverse to the first opening, and using at least one of the mask openings to define the location of a conductor to which the via or contact is to be connected ,further comprising etching a trench having a bottom in a dielectric using at least one of the openings with no etch stop layer formed on the bottom of the trench.

15. (Previously presented) The process of claim 1 wherein the second opening is perpendicular to the first opening.

16. (Previously presented) The process of claim 13 wherein the second opening is perpendicular to the first opening.

17. (Previously presented) The process of claim 14 wherein the second opening is perpendicular to the first opening.